## AMENDMENTS TO THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Claim 1 (Currently Amended): Within a programmable logic device, a routing architecture to interconnect a plurality of function blocks, comprising:

a plurality of wires oriented in a first direction for transmitting signals between the function blocks, wherein the wires oriented in the first direction have a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations.

Claim 2 (Currently Amended): The routing architecture of claim 1, further comprising a plurality of wires oriented in a second direction for transmitting signals between the function blocks, wherein the physical length of the wires oriented in the first direction is substantially the same as a physical length of the wires oriented in the second direction.

Claim 3 (Currently Amended): The routing architecture of claim 1 wherein the non-electrical considerations include at least one of the routing efficiency of the wires at the electrically optimum physical length and the pattern of connections to the ~~wire~~ wires.

Claim 4 (Currently Amended): The routing architecture of claim 1, further comprising a plurality of wires oriented in a second direction for transmitting signals between the function blocks, wherein the physical length of the wires oriented in the first direction substantially differs from a physical length of the wires oriented in the second direction.

Claim 5 (Previously Presented): The routing architecture of claim 1 wherein the first direction is substantially orthogonal to the second direction.

Claim 6 (Original): The routing architecture of claim 5 wherein the first direction and the second direction are any one of a horizontal direction and a vertical direction, the vertical direction and the horizontal direction, a diagonal direction up to the right and a diagonal direction up to the left, or the diagonal direction up to the left and the diagonal direction up to the right.

Claim 7 (Currently Amended): The routing architecture of claim 1 wherein each of the plurality of function blocks ~~are~~ is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

Claim 8 (Original): A digital system including the programmable logic device of claim 1.

Claim 9 (Original): Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a wire having a logical length that is a function of an orientation of the wire and having a physical length that is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations,

wherein the wire interconnects a subset of the plurality of function blocks.

Claim 10 (Original): The two-dimensional routing architecture of claim 9 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the electrically optimum physical length and the pattern of connections to the wire.

Claim 11 (Original): The two-dimensional routing architecture of claim 9 wherein the orientation of the wire is any one of a vertical direction, a horizontal direction, a diagonal direction up to the left, or a diagonal direction up to the right.

Claim 12 (Currently Amended): The two-dimensional routing architecture of claim 9 wherein each of the plurality of function blocks ~~are~~ is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

Claim 13 (Original): The two-dimensional routing architecture of claim 9 wherein each of the plurality of function blocks has a height that differs from its width.

Claim 14 (Original): A digital system including the programmable logic device of claim 9.

Claim 15 (Currently Amended): A method to interconnect a plurality of function blocks within a programmable logic device, comprising:

determining a physical length that is electrically optimum for a wire; ~~and~~

providing the wire having a physical length that is substantially the same as the determined physical length; and

connecting the plurality of function blocks to the wire ~~having a physical length that is substantially the same as the physical length that is electrically optimum,~~

wherein a logical length of the wire is a function of an orientation of the wire.

Claim 16 (Currently Amended): The method of claim 15 further comprising

adjusting the determined physical length to account for non-electrical considerations before providing the wire[[,]]

~~wherein connecting the plurality of function blocks is connecting to the wire having the physical length that is substantially the same as the adjusted physical length.~~

Claim 17 (Original): The method of claim 16 wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the physical length that is electrically optimum and the pattern of connections to the wire.

Claim 18 (Original): The method of claim 15 wherein determining the physical length that is optimum for the wire includes

modeling the programmable logic device that includes the plurality of function blocks and the wire;

varying the physical length of the wire a plurality of times;

for each of the plurality of physical length variations, determining the time for a signal to traverse the wire having the particular one of the plurality of physical length variations;

for each of the plurality of times for the signal to traverse the wire having the particular one of the plurality of physical length variations, converting this time to the time for the signal to traverse one unit length; and

from the plurality of times for the signal to traverse one unit length, selecting a particular one of the plurality of times for the signal to traverse one unit length that is the least time to traverse one unit length.

Claim 19 (Currently Amended): The method of claim 15 wherein each of the plurality of function blocks are is a logic array block, a memory block, an input/output block, or a multiply-accumulate block.

Claim 20 (Currently Amended): Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a first subset of a plurality of wires having a first logical length and a physical length for transmitting signals between the function blocks; and

a second subset of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of the plurality of wires for transmitting signals between the function blocks, wherein

the first logical length differs from the second logical length, and

the physical length of the first subset of the plurality of wires is substantially the same as an electrically optimum physical length or an adjustment of the electrically optimum physical length to account for non-electrical considerations.

Claim 21 (Previously Presented): The two-dimensional routing architecture of claim 20 wherein the physical length of the first subset of the plurality of wires is substantially the same as the physical length of the second subset of the plurality of wires.

Claim 22 (Previously Presented): The two-dimensional routing architecture of claim 20, wherein the non-electrical considerations include at least one of the routing efficiency of the wire at the physical length that is electrically optimum and the pattern of connections to the wire.

Claim 23 (Original): The two-dimensional routing architecture of claim 20 wherein the first subset of the plurality of wires is oriented in a first direction and the second subset of the plurality of wires is oriented in a second direction.

Claim 24 (Previously Presented): Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a first subset of a plurality of wires having a first logical length and a physical length;

a second subset of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of the plurality of wires, wherein the first logical length differs from the second logical length, and the first subset of the plurality of wires is oriented in a first direction and the second subset of the plurality of wires is oriented in a second direction;

a third subset of the plurality of wires oriented in the first direction and having a third logical length that is shorter than the first logical length;

a fourth subset of the plurality of wires oriented in the second direction and having the third logical length;

a fifth subset of the plurality of wires oriented in the first direction and having a fourth logical length that is shorter than the third logical length; and

a sixth subset of the plurality of wires oriented in the second direction and having the fourth logical length,

wherein a physical length of the third subset of the plurality of wires differs from a physical length of the fourth subset of the plurality of wires and a physical length of the fifth subset of the plurality of wires differs from a physical length of the sixth subset of the plurality of wires.

Claim 25 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein the first direction is substantially orthogonal to the second direction.

Claim 26 (Original): The two-dimensional routing architecture of claim 25 wherein the first direction is a horizontal direction and the second direction is a vertical direction and the first logical length is 24 function blocks, the second logical length is 16 function blocks, the third logical length is 8 function blocks, and the fourth logical length is 4 function blocks.

Claim 27 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein a first one of the plurality of wires is oriented in a stagger direction and has a first starting point, a first ending point, and a stagger logical length;

a second one of the plurality of wires is oriented in the stagger direction and has a second starting point, a second ending point, and the stagger logical length; and

if the stagger direction is a horizontal direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by a fixed number of a plurality of columns of function blocks of an array of function blocks, or if the stagger direction is a vertical direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by the fixed number of a plurality of rows of function blocks of the array of function blocks.

Claim 28 (Original): The two-dimensional routing architecture of claim 27 wherein the fixed number is any one of zero, one, or two.

Claim 29 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein the first direction is a horizontal direction, a first wire of a particular one of the first subset of the plurality of wires, the third subset of the plurality of wires, or the fifth subset of the plurality of wires has a first starting point, and a second wire of the particular one of the subsets has a second starting point; and the architecture further comprises:

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire to the right;

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire to the left.

Claim 30 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein the second direction is a vertical direction, a first wire of a particular one of the second subset of the plurality of wires, the fourth subset of the plurality of wires, or the sixth subset of the plurality of wires has a first starting point, and a second wire of the particular one of the subsets has a second starting point; and the architecture further comprises:

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire in the upward direction;

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire in the downward direction.

Claim 31 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein

a first one of the plurality of wires is oriented in a stitching direction and has a signal flow direction, a stitching logical length, a first starting point, and a first ending point that is the stitching logical length away in the signal flow direction from the first starting point; and

a second one of the plurality of wires is oriented in the stitching direction and has the signal flow direction, the stitching logical length, a second starting point, and a second ending point that is the stitching logical length away in the signal flow direction from the second starting point; and the architecture further comprises:

a driver having an input and an output, the input coupled to the first one of the plurality of wires at a position ranging from the first starting point to the first ending point and the output coupled to the second one of the plurality of wires at the second starting point, to drive the signal on the second one of the plurality of wires in the signal flow direction from the second starting point to the second ending point.

Claim 32 (Original): The two-dimensional routing architecture of claim 31 wherein the input of the second driver is coupled to the first one of the plurality of wires at the first ending point.

Claim 33 (Previously Presented): The two-dimensional routing architecture of claim 24, wherein

a first one of the fifth subset of the plurality of wires oriented in the first direction is coupled to at least one of a first one of the first subset of the plurality of wires oriented in the first direction, a first one of the second subset of the plurality of wires oriented in the second direction, a first one of the sixth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the first one of the fifth subset of the plurality of wires;

a first one of the third subset of the plurality of wires oriented in the first direction is coupled to at least one of a first one of the fourth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the first one of the third subset of the plurality of wires;

a second one of the first subset of the plurality of wires oriented in the first direction is coupled to at least one of a second one of the fifth subset of the plurality of wires oriented in the first direction, a second one of the second subset of the plurality of wires oriented in the second direction, and a second one of the sixth subset of the plurality of wires oriented in the second direction;

a third one of the sixth subset of the plurality of wires oriented in the second direction is coupled to at least one of a third one of the first subset of the plurality of wires oriented in the first direction, a third one of the fifth subset of the plurality of wires oriented in the first direction, a third one of the second subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the third one of the sixth subset of the plurality of wires;

a second one of the fourth subset of the plurality of wires oriented in the second direction is coupled to at least one of a second one of the third subset of the plurality of wires oriented in the first direction, and a particular one of the plurality of function blocks spanned by the second one of the fourth subset of the plurality of wires; and

a fourth one of the second subset of the plurality of wires oriented in the second direction is coupled to at least one of a fourth one of the first subset of the plurality of wires oriented in the first direction, a fourth one of the fifth subset of the plurality of wires oriented in the first direction, and a fourth one of the sixth subset of the plurality of wires oriented in the second direction.

Claim 34 (Previously Presented): The two-dimensional routing architecture of claim 24, further comprising:

a plurality of rows and a plurality of columns of function blocks;

a first driver corresponding to a first one of the plurality of columns of function blocks and having at least one input and an output, the at least one input coupled to at least one of a first one of the first subset of the plurality of wires, a first one of the second subset of the plurality of wires, a first one of the sixth subset of the plurality of wires, an output of the first one of the plurality of columns of function blocks, and an output of a second one of the plurality of columns of function blocks that is adjacent to the first one of the plurality of columns of function blocks, and the output of the first driver coupled to a first one of the fifth subset of the plurality of wires;

a second driver corresponding to a third one of the plurality of columns of function blocks and having at least one input and an output, the at least one input coupled to at least one of a first one of the fourth subset of the plurality of wires, an output of the third one of the plurality of columns of function blocks, and an output of a fourth one of the plurality of columns of function blocks that is adjacent to the third one of the plurality of columns of function blocks, and the output of the second driver coupled to a first one of the third subset of the plurality of wires;

a third driver having at least one input and an output, the at least one input coupled to at least one of a second one of the fifth subset of the plurality of wires, a second one of the second subset of the plurality of wires, and a second one of the sixth subset of the plurality of wires, and the output of the third driver coupled to a second one of the first subset of the plurality of wires;

a fourth driver corresponding to a first one of the plurality of rows of function blocks and having at least one input and an output, the at least one input coupled to at least one of a third one of the first subset of the plurality of wires, a third one of the fifth subset of the plurality of wires, a third one of the second subset of the plurality of wires, an output of the first one of the plurality of

rows of function blocks, and an output of a second one of the plurality of rows of function blocks that is adjacent to the first one of the plurality of rows of function blocks, and the output of the fourth driver coupled to a third one of the sixth subset of the plurality of wires;

a fifth driver corresponding to a third one of the plurality of rows of function blocks and having at least one input and an output, the at least one input coupled to at least one of a second one of the third subset of the plurality of wires, an output of the third one of the plurality of rows of function blocks, and an output of a fourth one of the plurality of rows of function blocks that is adjacent to the third one of the plurality of rows of function blocks, and the output of the fifth driver coupled to a second one of the fourth subset of the plurality of wires; and

a sixth driver having at least one input and an output, the at least one input coupled to at least one of a fourth one of the first subset of the plurality of wires, a fourth one of the fifth subset of the plurality of wires, and a fourth one of the sixth subset of the plurality of wires, and the output of the sixth driver coupled to a fourth one of the second subset of the plurality of wires.

Claim 35 (Original): The two-dimensional routing architecture of claim 24 wherein

the first subset of the plurality of wires is wider than the third subset of the plurality of wires, the third subset of the plurality of wires is wider than the fifth subset of the plurality of wires, the second subset of the plurality of wires is wider than the fourth subset of the plurality of wires, and the fourth subset of the plurality of wires is wider than the sixth subset of the plurality of wires.

Claim 36 (Previously Presented): Within a programmable logic device, a two-dimensional routing architecture to interconnect a plurality of function blocks, comprising:

a first subset of a plurality of wires having a first logical length and a physical length;

a second subset of the plurality of wires having a second logical length and a physical length that is substantially the same as the physical length of the first subset of the plurality of wires, wherein the first logical length differs from the second logical length, and the first subset of the plurality of wires is oriented in a first direction and the second subset of the plurality of wires is oriented in a second direction;

a third subset of the plurality of wires oriented in the first direction and having a third logical length that is shorter than the first logical length; and

a fourth subset of the plurality of wires oriented in the second direction and having the third logical length,

wherein a physical length of the third subset of the plurality of wires differs from a physical length of the fourth subset of the plurality of wires.

Claim 37 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein the first direction is substantially orthogonal to the second direction.

Claim 38 (Previously Presented): The two-dimensional routing architecture of claim 37, wherein the first direction is a horizontal direction and the second direction is a vertical direction and the first logical length is 24 function blocks, the second logical length is 16 function blocks, the third logical length is 4 function blocks.

Claim 39 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein

a first one of the plurality of wires is oriented in a stagger direction and has a first starting point, a first ending point, and a stagger logical length;

a second one of the plurality of wires is oriented in the stagger direction and has a second starting point, a second ending point, and the stagger logical length; and

if the stagger direction is a horizontal direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by a fixed number of a plurality of columns of function blocks of an array of function blocks, or if the stagger direction is a vertical direction then the first starting point is offset from the second starting point and the first ending point is offset from the second ending point by the fixed number of a plurality of rows of function blocks of the array of function blocks.

Claim 40 (Previously Presented): The two-dimensional routing architecture of claim 39, wherein the fixed number is any one of zero, one, or two.

Claim 41 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein the first direction is a horizontal direction, a first wire of a particular one of the first subset of the plurality of wires or the third subset of the plurality of wires has a first starting point, and a second wire of the particular one of the subsets has a second starting point; and the architecture further comprises:

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire to the right; and

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire to the left.

Claim 42 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein the second direction is a vertical direction, a first wire of a particular one of the second subset of the plurality of wires or the fourth subset of the plurality of wires has a first starting point, and a second wire of the particular one of the subsets has a second starting point; and the architecture further comprises:

a first driver having an output, the output coupled to the first wire at the first starting point, to drive a first signal on the first wire in the upward direction; and

a second driver having an output, the output coupled to the second wire at the second starting point, to drive a second signal on the second wire in the downward direction.

Claim 43 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein

a first one of the plurality of wires is oriented in a stitching direction and has a signal flow direction, a stitching logical length, a first starting point, and a first ending point that is the stitching logical length away in the signal flow direction from the first starting point; and

a second one of the plurality of wires is oriented in the stitching direction and has the signal flow direction, the stitching logical length, a second starting point, and a second ending point that is the stitching logical length away in the signal flow direction from the second starting point; and the architecture further comprises:

a driver having an input and an output, the input coupled to the first one of the plurality of wires at a position ranging from the first starting point to the first ending point and the output coupled to the second one of the plurality of wires at the second starting point, to drive the signal on the second one of the plurality of wires in the signal flow direction from the second starting point to the second ending point.

Claim 44 (Previously Presented): The two-dimensional routing architecture of claim 43, wherein the input of the second driver is coupled to the first one of the plurality of wires at the first ending point.

Claim 45 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein a first one of the third subset of the plurality of wires oriented in the first direction is coupled to at least one of a first one of the first subset of the plurality of wires oriented in the first direction, a first one of the second subset of the plurality of wires oriented in the second direction, a first one of the fourth subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the first one of the third subset of the plurality of wires;

a second one of the first subset of the plurality of wires oriented in the first direction is coupled to at least one of a second one of the third subset of the plurality of wires oriented in the first direction, a second one of the second subset of the plurality of wires oriented in the second direction, and a second one of the fourth subset of the plurality of wires oriented in the second direction;

a third one of the fourth subset of the plurality of wires oriented in the second direction is coupled to at least one of a third one of the first subset of the plurality of wires oriented in the first direction, a third one of the third subset of the plurality of wires oriented in the first direction, a third one of the second subset of the plurality of wires oriented in the second direction, and a particular one of the plurality of function blocks spanned by the third one of the fourth subset of the plurality of wires; and

a fourth one of the second subset of the plurality of wires oriented in the second direction is coupled to at least one of a fourth one of the first subset of the plurality of wires oriented in the first

direction, a fourth one of the third subset of the plurality of wires oriented in the first direction, a fourth one of the fourth subset of the plurality of wires oriented in the second direction.

Claim 46 (Previously Presented): The two-dimensional routing architecture of claim 36, further comprising:

a plurality of rows and a plurality of columns of function blocks;

a first driver corresponding to a first one of the plurality of columns of function blocks and having at least one input and an output, the at least one input coupled to at least one of a first one of the first subset of the plurality of wires, a first one of the second subset of the plurality of wires, a first one of the fourth subset of the plurality of wires, an output of the first one of the plurality of columns of function blocks, and an output of a second one of the plurality of columns of function blocks that is adjacent to the first one of the plurality of columns of function blocks, and the output of the first driver coupled to a first one of the third subset of the plurality of wires;

a second driver having at least one input and an output, the at least one input coupled to at least one of a second one of the third subset of the plurality of wires, a second one of the second subset of the plurality of wires, and a second one of the fourth subset of the plurality of wires, and the output of the third driver coupled to a second one of the first subset of the plurality of wires;

a third driver corresponding to a first one of the plurality of rows of function blocks and having at least one input and an output, the at least one input coupled to at least one of a third one of the first subset of the plurality of wires, a third one of the third subset of the plurality of wires, a third one of the second subset of the plurality of wires, an output of the first one of the plurality of rows of function blocks, and an output of a second one of the plurality of rows of function blocks that is adjacent to the first one of the plurality of rows of function blocks, and the output of the fourth driver coupled to a third one of the fourth subset of the plurality of wires; and

a fourth driver having at least one input and an output, the at least one input coupled to a at least one of fourth one of the first subset of the plurality of wires, a fourth one of the third subset of the plurality of wires, and a fourth one of the fourth subset of the plurality of wires, and the output of the sixth driver coupled to a fourth one of the second subset of the plurality of wires.

Claim 47 (Previously Presented): The two-dimensional routing architecture of claim 36, wherein the first subset of the plurality of wires is wider than the third subset of the plurality of wires, the second subset of the plurality of wires is wider than the fourth subset of the plurality of wires.